

LSI Docket No. 03-1597

Remarks/Arguments

In the Office Action mailed on 1 June 2005, the Examiner rejected all claims 1-19 under 35 U.S.C. §102(b) as anticipated by Matsushita (United States Patent Number 6,504,270).

Applicants respectfully traverse the Examiner's §102 rejection and have amended various claims for editorial clarity and to better protect the invention.

§102 Rejections

The Examiner rejected all claims 1-19 under §102 as anticipated by Matsushita. The Examiner does not cite specific features of specific claims as read in the teachings of Matsushita but generally points to various components of the circuits of Matsushita shown in figures 1-7 as showing each feature of the rejected claims. In particular, looking initially at only claim 1, the Examiner points to the recited AC input stage as Matsushita's AC voltage 1, the recited DC input stage as Matsushita's battery voltage 26, and does not specifically identify any element of Matsushita as the recited DC output stage. In like manner, similar structures and related method steps recited by independent claims 10 and 18 are no more clearly identified.

Even accepting, *arguendo*, the Examiner's reading of these elements of rejected claim 1 ignores the additional structure recited in, for example, rejected claim 7 (dependent from claim 1). The Examiner's reading of a DC input stage as battery 26 does not teach the recited additional elements of the recited DC input stage of, for example, claim 7. Specifically, battery 26 of Matsushita (read by the Examiner as the DC input stage) does not include the recited switching circuit element, the recited transformer, and the recited full-wave rectifier circuit - all elements of the DC input stage as recited in rejected claim 7. The Examiner suggests such elements are present in the various figures of Matsushita reading the switching circuit as element 69, a transformer as element 22 and the rectifier as element 4. This reading simply ignores the recited structure of, for example, claim 7 wherein these elements are part of the DC input stage. In other words, the Examiner's reading of battery 26 as the recited DC input stage cannot be read as including these other elements scattered through other circuits of Matsushita's structures.

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Despite this lack of clarity, Applicant acknowledges a more reasonable understanding of Matsushita as teaching an AC input stage as element 21 of his figure 1, a DC input stage as element 69, and a DC output stage as element 25 of his figure 1. Even under this more reasonable reading of Matsushita, the DC input stage element 69 of Matsushita's figure 1 et seq. still does not show the additional recited structure of, for example, rejected claim 7. Simply put, the structure of the DC input stage as recited in, for example, rejected claim 7 is neither shown by Matsushita nor reasonably suggested thereby. The DC input stage 69 of Matsushita simply does not convert the DC input supply voltage (i.e., of battery 26) to an AC waveform and then rectify that generated AC signal to a DC voltage applied to the DC output stage. The elements cited by the Examiner are not part of a DC input stage. In particular, rectifier 4 of Matsushita has nothing to do with rectifying an AC waveform generated from the DC input source voltage (battery 26 of Matsushita) nor any portion of the DC input stage (69 of Matsushita). Rather, rectifier 4 of Matsushita rectifies the AC input source voltage 1.

In hopes of advancing the prosecution of this patent application, Applicant has amended claim 1 to integrate the essential elements of rejected claim 7 and has therefore cancelled claim 7. Applicant therefore maintains that rejected claim 1, as amended, is allowable over Matsushita and all art of record (considered individually or in any combination).

Claim 8 as filed was dependent from claim 1 and includes limitations similar to that of claim 7 but adding a buffer circuit to provide electrical current to the AC waveform. Claim 8 has been amended to correct its recitation in view of the common features of claim 7 being amended into claim 1.

In like manner, independent claim 10 has been amended to incorporate essential elements of rejected claim 15 which recites additional features of the DC input stage. Rejected independent method claim 18 already includes recitations of receiving DC electrical power in a DC input stage, converting the DC power to an AC waveform, transforming the AC waveform to another AC voltage and rectifying that resulting AC voltage. These method steps are nowhere taught in the structure or operation of

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Matsushita (whether reading the DC input stage as battery 26 as suggested by the Examiner or as input stage 69 as suggested by Applicant). Applicant therefore maintains that claim 10 as amended and claim 18 as amended are allowable over the teachings of Matsushita.

Claim 16 as filed was dependent from claim 10 and includes limitations similar to that of claim 15 but adding a buffer circuit to provide electrical current to the AC waveform. Claim 16 has been amended to correct its recitation in view of the common features of claim 15 being amended into claim 10.

Claim 19 has been amended to correct a typographic error. Applicant therefore maintains that all remaining dependent claims (2-6, 8, 11-14, 16, and 19) are allowable for at least the same reasons as discussed above and as dependent from allowable base claims. Applicant respectfully requests reconsideration and withdrawal of the rejection of all remaining claims 1-6, 8-14, and 16-19.

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Conclusion

Applicants have amended claims 1 and 10 to overcome the Examiner's rejection and have cancelled claims 7 and 15. Other claims have been amended to correct dependencies and other typographic errors. Applicant has thoroughly discussed the Examiner's §102 rejection, have traversed that rejection and have requested reconsideration and withdrawal of same.

No additional fees are believed due. Should any issues remain, the Examiner is encouraged to telephone the undersigned attorney.

Respectfully submitted,



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